28 GHz Band High Linearity Frequency Conversion IC for 5G Mobile Communication Systems

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Phased array antenna modules can benefit from scalability, configurability and Si area efficiency by splitting beamforming and frequency conversion functions between separate ICs. This paper introduces a frequency conversion IC having high-linearity and architectural features that enables to support dual-polarized, scalable phased arrays with >64 antenna elements for the mm-wave 5G systems.

1. Introduction

Scalable phased arrays for millimeter wave band is the key technology for high-data rate 5G mobile communication systems. Phased array modules incorporate both beamforming circuits as well as frequency conversion circuits to interface between antenna array and the IF signal. Frequency conversion between RF and IF signals is sometimes included in beamforming IC (BFIC) and therefore shared among multiple antenna elements [1) 2) 3) 4) 5)]. And this type of BFICs are to form a large scale tiled array where IF and LO signals are to be provided to each IC [4)]. Though this configuration does not require RF signal distribution to each IC, it needs power and area for frequency conversion circuit in each IC. In addition, IF and LO distribution should be phase-aligned with all ICs. On the other hand, there is another approach that distributes RF signals throughout the tiled-array around a single frequency conversion IC (FCIC) [5)]. This approach, however, needs to handle the combined RF signal coming from all the front-ends in receive mode, which shall be challenging to meet the linearity requirements of RX chain as one of the key design specifications [6)]. If RF channel filter is not available, the linearity will be highly

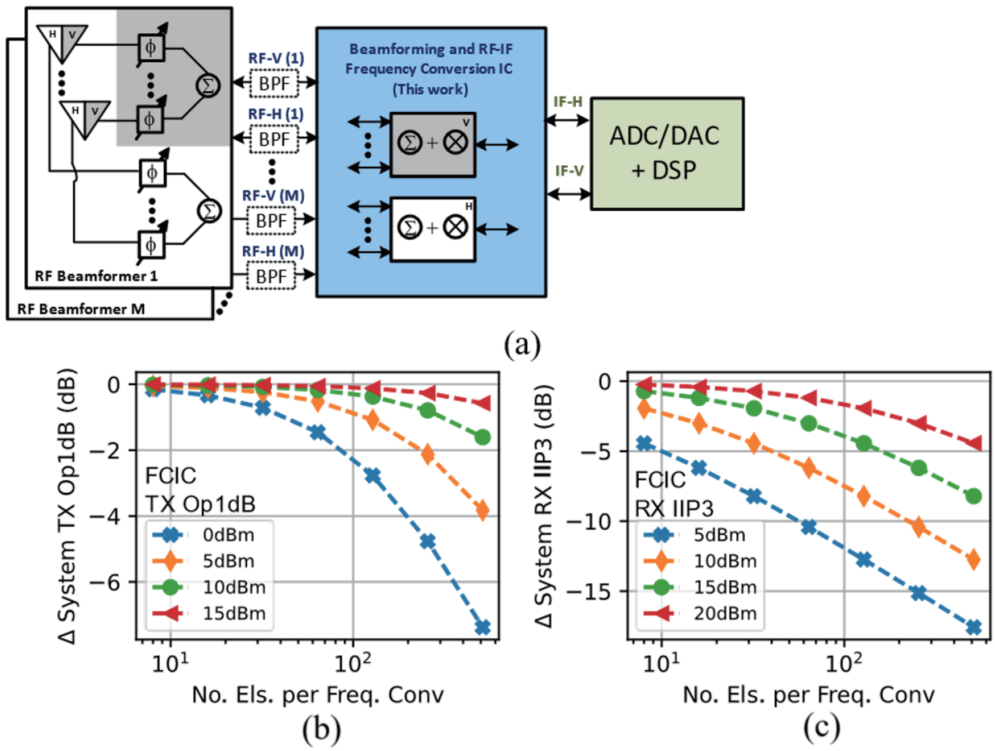


Fig. 1. (a) Scalable phased array architecture with BFICs and FCICs. (b) Degradation in phased array TX OP1dB/output vs. # array elements supported / RF port for four values of FCIC OP1dB/RF port (c) Degradation in phased array RX IIP3 vs. # array elements for four values of FCIC IIP3/RF port [8)].

Abbreviations, Acronyms, and Terms.

5G—Fifth Generation Mobile Communication System
The fifth-generation technology standard for broadband cellular networks.

Phased Array Antenna—Phased Array Antenna
An array of antennas which creates a beam of radio waves that can be electronically steered to point in different directions without moving the antennas.

Beamforming—Beamforming
Creating a beam of radio waves by combining elements in an antenna array.

Dual Polarization—Dual Polarization
Radio waves in both a horizontal and vertical orientation.

RF—Radio Frequency
A frequency that can be used as a carrier wave for wireless communications. Generally refers to the range from 300Hz to 3THz.

LO—Local Oscillator
Local oscillator, or its frequency of oscillation. Used for frequency conversion as a reference signal for heterodyne receivers.

IF—Intermediate Frequency
A frequency to which a carrier wave is shifted as an intermediate step in transmission or reception.

Conversion Gain—Conversion Gain
Gain in circuits such as mixers with different input and output frequencies.

P1dB—1dB Compression Point
One of the key performance metrics that indicate the linearity of an amplifier. The input or output point at 1 dB below the small signal gain. The output point is often notated as OP1dB and the input point as IP1dB.

IM3—3rd Order Inter-Modulation Distortion
Harmonic distortion that occurs between one fundamental wave and the second harmonic of another wave when the two waves are close in frequency, and applied simultaneously to a nonlinear system. It cannot be removed by a filter because its frequency is too close to the fundamental wave.

IP3—3rd Order Intercept Point
One of the key performance metrics that indicate the linearity of an amplifier. The calculated point at which IM3 equals the fundamental wave. The output point is notated as OIP3, and the input point as IIP3.

NF—Noise Figure
The ratio of a circuit's input S/N ratio to its output S/N ratio.

Up Conversion Mixer—Up Conversion Mixer
A circuit that mixes a low frequency signal such as an IF signal and an LO signal and converts it to a high frequency signal such as an RF signal.

Down Conversion Mixer—Down Conversion Mixer
A circuit that mixes a high frequency signal such as an RF signal and an LO signal and converts it to a low frequency signal such as an IF signal.

Double Balanced Mixer—Double Balanced Mixer
A mixer topology that suppresses the leakage of the input signals to the output port.

Gilbert Cell—Gilbert Cell
One of double-balanced mixers composed of transistors.

Balun—Balun—A circuit that converts differential signals to a single-ended signal or vice versa.

CMOS—Complementary MOS
Semiconductor circuits based on P-type and N-type MOS transistors, or their manufacturing technology.

BiCMOS—Bipolar CMOS
A semiconductor circuit that uses bipolar transistor circuits and CMOS circuits, or its manufacturing technology.

EM Simulation—Electromagnetic Simulation
An approach to the analysis of electric and magnetic fields in space or matter. There are the FDTD method calculated in the time domain, and the Moment method and the FEM method calculated in the frequency domain.

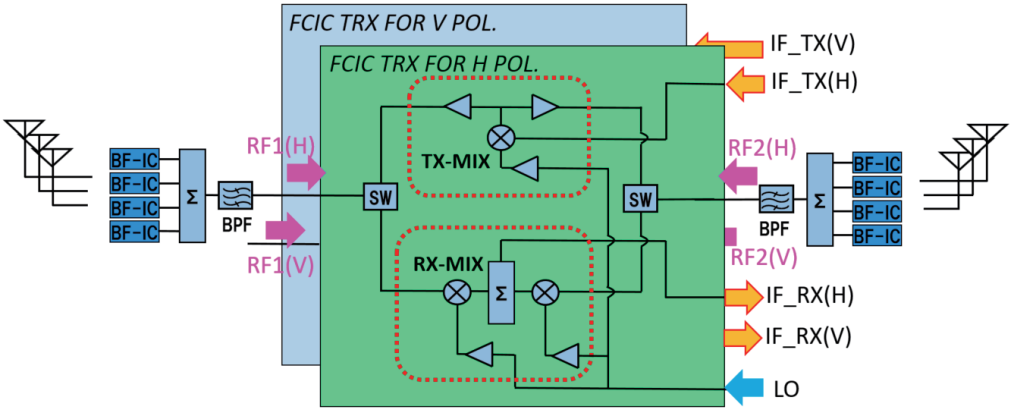
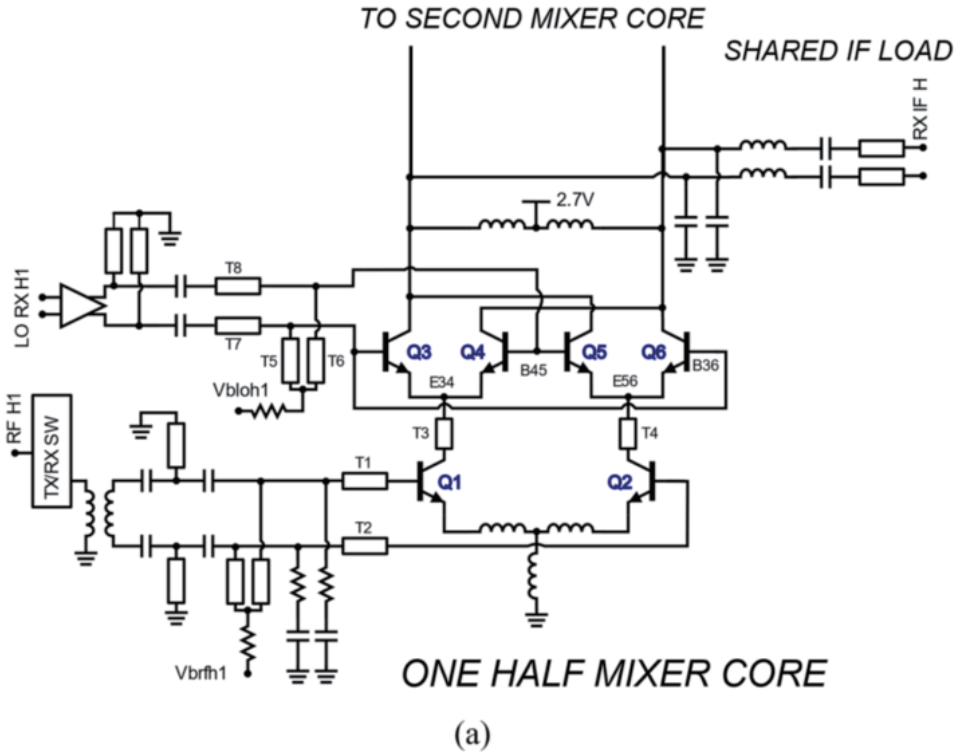


Fig. 2. Configuration of the Proposed FCIC.



(a)

Fig. 3. Schematics of the proposed down-conversion mixer.

challenging for wide-band phased arrays in the presence of in-band interferers.

In this paper, we introduce the design, architecture and performance of a high-linearity FCIC. A single FCIC can be shared among multiple BFICs and then the whole can be integrated into an antenna array in package [7] which then further can form a scaled phased array as shown in Fig. 1 (a) [8]. A system-level linearity analysis performed by Paidimarri et al.[8] shows how much linearity FCIC requires per RF port to support multiple antenna elements. (Fig. 1 (b) and 1 (c))

In transmit (TX) path (Fig. 1 (b)), at the system level, the output 1 dB gain compression point (OP1 dB) is degraded by 0.2 dB for 64 elements per RF port when OP1dB of FCIC is +10 dBm. The TX OP1dB of FCIC could be moderate with higher front-end gain in BFIC so long as the stability of BFIC is ensured in TX mode. In receive (RX) path (Fig. 1 (c)) at system level, the input third-order intercept point (IIP3) is degraded by 3 dB for 64 elements per RF port when IIP3 of FCIC is +15 dBm. RX mixer linearity requirement of FCIC could be moderate with lower front end gain in BFIC while noise figure (NF) is degraded as the system level. When the number of phased array elements per BFIC RF port is (N), by just increasing the number of RF ports (M) of FCIC, the total number of phased array elements (N x M) can be increased without compromising system linearity.

2. IC Configuration

Figure 2 shows the proposed FCIC configuration which supports dual polarization operation with two RF ports (M = 2) while achieving high linearity over the RF frequency range of 24 to 30 GHz and the IF frequency range of 2 to 5 GHz. TX chain is composed of an up-conversion mixer, a power splitter, two power amplifiers and TX / RX

switches. TX chain needs high OP1dB (~ +10 dBm) and high gain (> +25 dB) to support more than 64 phased array elements at each RF port. RX chain is composed of two TX / RX switches, two down-conversion mixers, and an IF power combiner to combine power from two RF ports. RX chain needs high IIP3 (> +14 dBm), moderate NF (~ +14 dB) and low gain (~0 dB) so that more than 64 phased array elements can be supported at each RF port. While sharing a single FCIC among many BFICs, external band-pass filters have to be placed between FCIC and BFICs for image suppression.

3. Up Conversion Mixer Design

The TX path utilizes a double balanced Gilbert cell mixer for up-converting IF signal (from 2 to 5 GHz) to RF signal. The external band pass filter suppresses the image frequency. This approach can avoid design challenges to implement wideband LO and IF quadrature generation or multi-stage up-conversion [3]. The IF input uses resistive matching for wideband IF matching. The RF output uses a capacitor with a low Q value for wideband RF matching. The conversion gain of the mixer alone is about +6 dB. The output signal of the mixer is distributed to two PAs through a transmission line-based splitter. Each PA has a gain of +23 dB over the RF range of 21 to 30 GHz.

4. Down Conversion Mixer Design

Figure 3 shows a simplified circuit diagram of the RX path. RX path receives two RF inputs corresponding to different beamforming paths. A single-ended RF signal is converted to differential signals by passive transformer with a coupling factor of 0.8. The insertion loss is less than +1.5 dB. Phase imbalance and insertion loss difference between differential outputs is less than 2 degrees and 0.1 dB respectively from 24 to 30 GHz. The input differential pair of each mixer core is degenerated by a differential inductor, and a common mode inductor to the ground. These two inductors improve input impedance matching as well as common mode rejection. Mixer input return loss is less than -10 dB from 23 to 31 GHz. Two mixer cores share one differential inductor load to enable both power supply biasing and current combining of the two mixer outputs at one IF output.

One of the most important challenges in down-conversion mixer design is high linearity to support more than 64 antenna elements per RF port. This goal is achieved architecturally by combining the IF at mixer output rather than combining RF at the mixer input. IIP3 needs more than +10 dBm for each mixer core. Comparable linearity at millimeter waves has recently been demonstrated using third order modulation suppression techniques. However they are validated at just a single frequency and at specific range of input power levels [6) 11)].

The down-conversion mixer utilizes large-size transistors for RF differential inputs (80 μm) and LO switching quad (64 μm) in order to achieve high linearity across wide RF bandwidth. This design approach is effective to linearity enhancement, however, it brings a possible instability issue because a long interconnect between large devices produces parasitic inductance and the transistors still have gain at higher frequency. In order to avoid unwanted instability, LO and RF input impedance matching network is co-designed and modelled precisely with interconnect devices around large-size transistors. For designing the interconnections between transistors, electromagnetic simulations were performed up to 200 GHz on a 94-port model.

5. Performances

The FCIC is fabricated using 130 nm SiGe BiCMOS technology. It has an area of 2.3 x 4.6 mm2. Figure 4 shows the fabricated FCIC capable of supporting two polarizations with a common LO input. Each polarization has two RF ports. The TX power-amplifiers are powered by 1.5 V while the TX up-conversion mixer and RX down-conversion mixer are powered by 2.7 V.

5.1. Transmit Mode

In TX mode, the current consumption is 47 mA (2.7 V) and 85 mA (1.5 V) per polarization. LO input power is -2 ± 1 dBm across the LO frequency range. The conversion gain is 27 dB or more across RF frequency range. OP1dB is more than +7 dBm and up to +10.2 dBm.

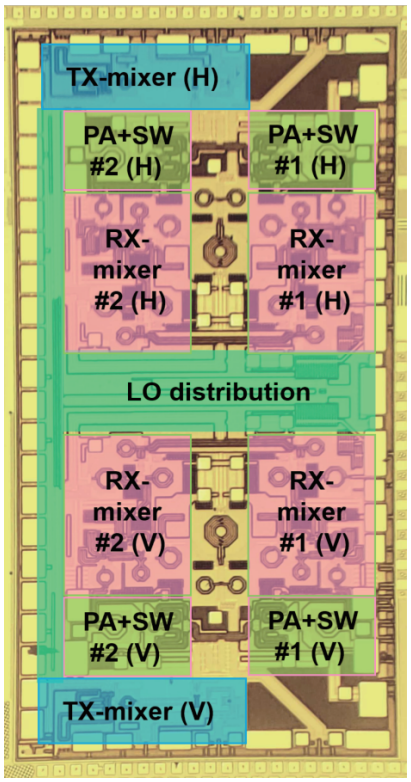


Fig. 4. Photo of the fabricated FCIC .

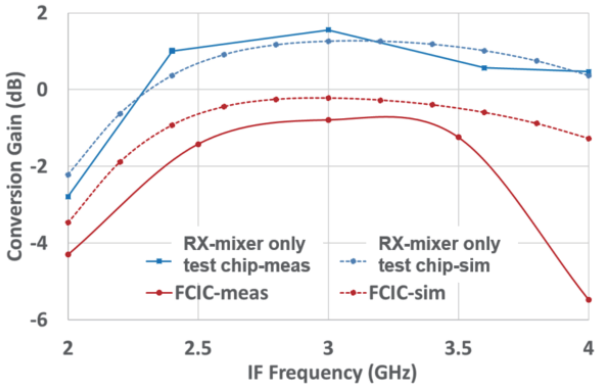


Fig. 5. Small signal frequency response of FCIC and RX mixer-only test chip (LO frequency is 25 GHz and LO power is 0 dBm).

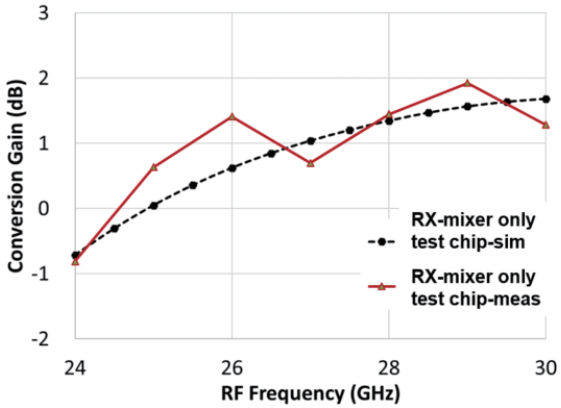


Fig. 6. Conversion gain of RX mixer-only test chip with 3 GHz IF and Δf=50 MHz.

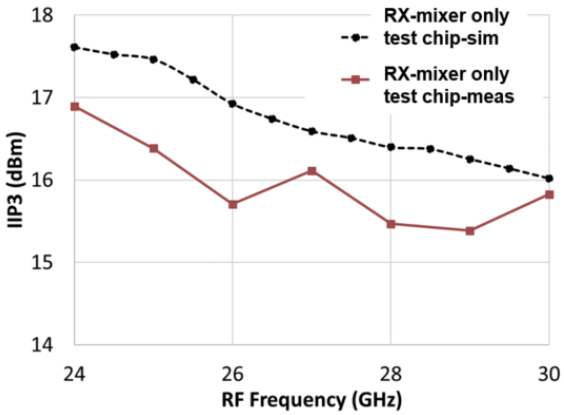


Fig. 7. IIP3 of RX mixer-only test chip with 3 GHz IF and Δf=50 MHz.

5.2. Receive Mode

In RX mode, the current consumption is 78 mA (2.7 V). Figure 5 shows conversion gain when RF frequency is from 27 to 29 GHz, LO frequency is 25 GHz, LO input is 0 dBm, and IF frequency is from 2 to 4 GHz. The linearity is measured on test chip ICs including mixer-cores-only while one of mixer-cores is active. Figure 6 and 7 show conversion gain and IIP3 respectively when RF frequency is from 24 to 30 GHz, LO frequency is from 21 to 27 GHz, LO input is +5 dBm, and IF frequency is 3 GHz. Small signal conversion gain is from –1 to +2 dB. IIP3 (Δf = 50 MHz) is +14.5 dBm or more over the RF frequency range. The conversion gain of the mixer-core-only IC is approximately +1.5 dB higher than the FCIC, which is consistent with the simulation results.

Table 1. A Summary of the proposed FCIC.

Polarizations	2
RF ports / Pol.	2
Antenna elements / RF ports	> 64
Frequency Range (GHz)	24-30 (RF), 2-5 (IF)
Technology	130nm SiGe BiCMOS
Chip area (mm^2)	10.6
Chip area / Antenna elements (mm^2)	0.41

Table 2. A Summary of Measured Performances.

Measurements	TX Mode	RX Mode
Conversion Gain (dB)	> 27	-1
Noise Figure (dB)	< 12.5	< 15
OP1dB (dBm)	7 to 14	6
IIP3 (dBm)		> 14.5
Power / RF ports (mW)	215	210
Power / Antenna elements (mW)	3.4	3.3

6. Conclusion

This paper introduces an FCIC with the capability of scaled phased array implementation. By implementing the frequency conversion function as a single IC outside the BFIC, the requirement of LO and IF signal distribution and phase synchronization is significantly relaxed for tiling larger arrays. In addition, the power consumption and IC areas are also reduced since the number of FCIC is smaller in a scaled phased array implementation.

Measurements confirmed that RX chain IIP3 is +14.5 dBm or more, TX chain OP1dB is from +7 to +14 dBm, and showed that the proposed FCIC can support more than 64 phased array elements per RF port. The proposed FCIC is designed for wideband operation over the RF frequency range of 24 to 30 GHz. Tables 1 and 2 show that the power consumption is 215 mW (TX or RX) and the the chip area is 2.65 mm^2 per RF port. Also, the power consumption is 3.4 mW and the area is 0.041 mm^2 per array element.

Reference

1) H.-C. Park et al.: "A 39GHz Band CMOS 16-Channel Phased-Array Transceiver IC with a Companion Dual-Stream IF transceiver IC for 5G NR Base-Station Applications", 2020 IEEE International Solid-State Circuits Conference, pp. 76-78, Feb. 2020.
2) J. D. Dunworth et al.: "A 28GHz Bulk-CMOS Dual-Polarization Phased-Array Transceiver with 24 Channels for 5G User and Basestation Equipment", 2018 IEEE International Solid- State Circuits Conference, pp. 70-71, Feb. 2018.
3) B. Sadhu et al.: "A 28-GHz 32-Element TRX Phased-Array IC with Concurrent Dual-Polarized Operation and Orthogonal Phase and Gain Control for 5G Communications", IEEE Journal of Solid-State Circuits, Vol. 52, No.12, pp. 3373-3391, Dec. 2017.
4) S. Shahramian, et al.: "A Fully Integrated 384-Element, 16-Tile, W-Band Phased Array with Self-Alignment and Self-Test", IEEE Journal of Solid-State Circuits, vol. 54, no. 9, pp. 2419-2434, Sept. 2019.
5) T. Sowlati et al.: "A 60-GHz 144-Element Phased-Array Transceiver for Backhaul Application", IEEE Journal of Solid-State Circuits, Vol. 53, No.12, pp. 3640-3659, Dec. 2018.
6) C. Chen, et al.: "38-GHz CMOS Linearized Receiver with IM3 Suppression, P1 dB/IP3/RR3 Enhancements, and Mitigation of QAM Constellation Diagram Distortion in 5G MMW Systems", IEEE Transactions on Microwave Theory and Techniques, Vol. 68, No. 7, pp. 2779-2795, July 2020.
7) X. Gu et al.: "Antenna-in-Package Integration for a Wide-Band Scalable 5G Millimeter-Wave Phased-Array Module," IEEE Microwave and Wireless Components Letters, Vol.31, Issue 6, pp.682-684, June. 2021.
8) A. Paidimarri, et al.: "A High-Linearity, 24–30 GHz RF, Beamforming and Frequency-Conversion IC for Scalable 5G Phased Arrays", 2021 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), pp.103-106, June. 2021.
9) Y. Uemichi et al.: "Highly Configurable Cylindrical-Resonator-Based Bandpass Filter Built of Silica-Based Post-Wall Waveguide and Its Application to Compact E-Band Hybrid-Coupled Diplexer," IEEE MTT-S International Microwave Symposium (IMS), pp. 726-729, June. 2019.
10) Y. Hasegawa, et al.:" Compact and Low-loss Stripline Band-pass Filter Made of Liquid Crystal Polymer for n257 and n258 Application," 51st European Microwave Conference, to be published.
11) C.-L. Wu, et al.: "Amplification of Nonlinearity in Multiple Gate Transistor Millimeter Wave Mixer for Improvement of Linearity and Noise Figure", IEEE Microwave and Wireless Components Letters, Vol.25, No.5, pp. 310-312 May. 2015.