High Aspect Ratio Through-hole Interconnections in Silicon Substrates

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We have developed key technologies to form conductive interconnections through a thick silicon substrate, which are potentially applied for 3D stacking of semiconductor devices or packaging of Micro Optical Electro-Mechanical System devices. In this paper, we demonstrate to form metal filled through-holes in thick Silicon substrates (t = ~500μm) mainly using Photo Assisted Electro-Chemical Etching and Molten Metal Suctioned Method. The through-holes had 15 μm in the diameter and the aspect ratio of 35. And the maximum density was 500 THs/cm^2. The dielectric breakdown voltage of the through-holes was more than 500V. In result of a radioisotope leak test using Kr-85, the leakage rate of through-holes between the front and the back of the substrate was lower than the limit of detection (1×10^{-15} Pa · m^3/sec.).

1. Introduction

Recently semiconductor devices, such as sensors, MPU and memory, have made dramatic progress in their integration and downsizing. New combination devices between optical ones and semiconductor ones, for instance, optical switches using micro mirrors and optical waveguides , are now being realized by means of Micro Electro-Mechanical System (MEMS) technology's advances. Under those backgrounds, the high-density system integration using the 3D stacking has been investigated aiming at further high speed and multi-function, lightweight and/or downsize. The 3D stacking using the conventional wire bonding technique has limits in the size and the number of IC chips can be stacked. Also stacking thin packaged devices with interposers has no limits in the number of the layer, but has longer wirings among elements. Conductive interconnections through Si substrates can solve the issues[1]. Fig. 1 shows our concept image of 3D stacking devices. In order to reduce the strain due to thermal expansion, we use Si as the material for the substrate of through-hole (TH) IC chips because Si is the same material as semiconductor devices. In addition, the excellent heat radiation capability of Si works in favor of mounting self-heat-generating devices such as MPU and laser diodes. On the other hand, even for single layer device, such as image sensors, which requires wider sensitive area in a die as much as it can be, the Si TH interconnections must be helpful to reduce package size because they can make terminal leads on the backside of the die.

In order to form conductive interconnections through a thick Si substrate, we have developed two key technologies, Photo Assisted Electro-Chemical Etching (PAECE) and Molten Metal Suctioned Method (MMSM). The PAECE can form high aspect ratio THs in a Si substrate, also the MMSM can fill many THs with a metal at once using vacuum pressure. The followings describe results of preparations for prototype samples using the two key technologies.

2. Process of Preparation

2.1 Forming TH

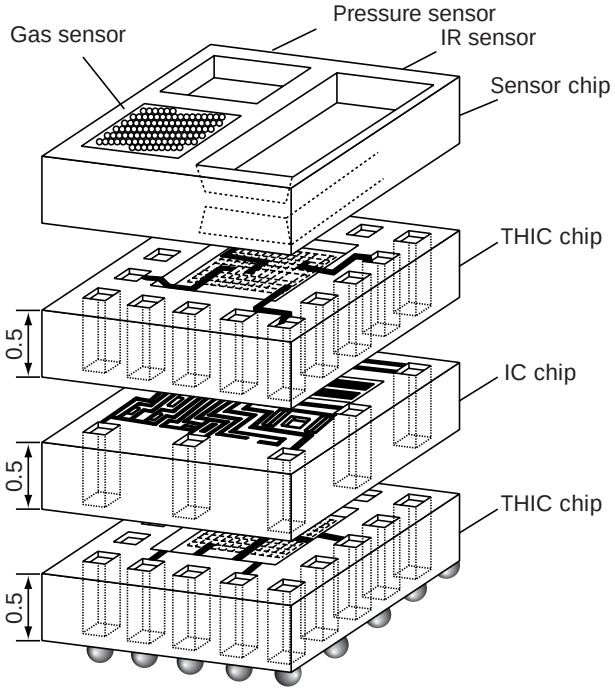

Fig. 1. Schematic View of 3D Stacking Devices.

2.1.1 PAECE [2) 3)]

PAECE is an anisotropic wet etching technology, which can form high aspect ratio THs. The principle of the PAECE is shown in Fig. 2. The front side of a Si wafer was exposed to 2.5wt% HF solution. A xenon lamp irradiated the backside surface of the wafer, and a band-pass filter, which passed lights of wavelengths between 370nm and 750nm, was placed in the optical path. The Si wafer, in which THs were to be formed, worked as the anode electrode and a Pt plate was set in HF electrolyte as cathode. V-grooves were formed certain places, where THs were needed, on the front surface of the wafer from the mask opening by anisotropic etching with KOH solution. The followings describe the mechanism of the PAECE. The minority carriers, positive holes in this case, are generated within a depth of approximately 11μm from the bottom surface, and move toward the front surface by the electric field applied between the anode and the cathode electrode. The concentration of electric field at the peak of the V-groove leads electric charges (positive holes), where the chemical reaction like equation (1) occurs and etches Si to form THs.

$Si + 6HF + 2hole(+) \rightarrow H_2SiF_6 + H_2 + 2H^+$ ····· (1)

Typical PAECE conditions are;

- Silicon substrate: n type, 525μm thickness and double side mirror polished Si wafer, of which direction was (100) grown by the Magnetic Czochralski (MCZ).
- Electrolyte: 2.5wt% HF solution
- Surfactant: 10wt% C_2H_5OH
- Temperature of electrolyte: 45~50°C
- Current density: 6~12mA/cm^2 (DC voltage = 0.5~2.0V)
- Light intensity: 5~100mW/cm^2

We succeeded to make 500THs/cm^2 in a thick Si substrate, each of which opening diameter was 13μm and the aspect ratio was 39. The etching rate was around 1.0μm/min. under the optimized conditions for good sidewall morphology of the TH. Fig. 3 shows the cross-sectional view of the THs.

2.1.2 Improving Sidewall Quality of THs

PAECE can make high aspect ratio THs, however the substrate must be n-type (100) and there is a major problem in its sidewall qualities. It is so-called 'side-branch', which is etching profile proceeding to a certain undesirable [010] and [001] directions. Fig. 4 shows another cross sectional view of THs made by PAECE. While the sidewall in the [110] cutting plane has good morphology, the 'side-branches' are clearly observed in the [001] and [010] planes at THs made in the same substrate. Through some experiments, we finally concluded the reason why the 'side-branches' were produced was that more dangling bonds of the [001] and [010] was attacked by HF solution and surplus holes compared to [110] direction's.

In order to minimize the 'side-branches', we have

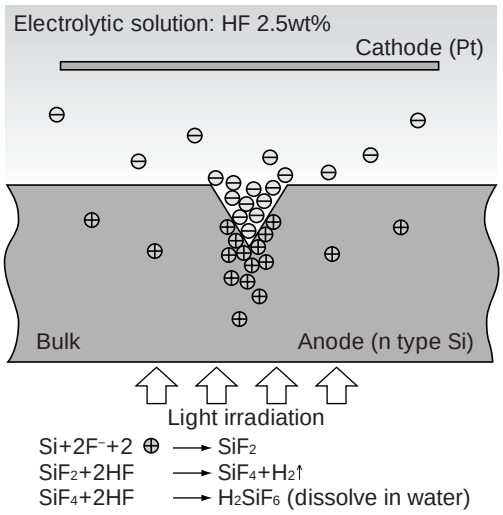

Fig. 2. Principle of PAECE.

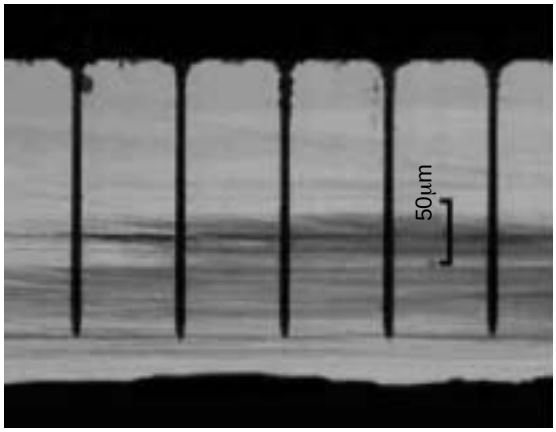

Fig. 3. Cross Sectional View of Through-holes in Silicon Substrate by PAECE.

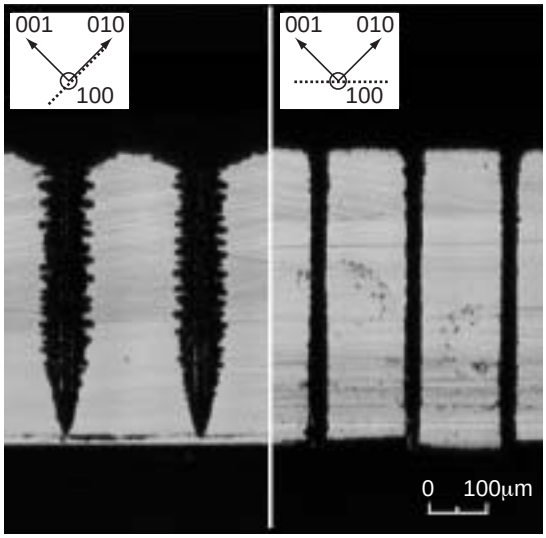

Fig. 4. Cross Sectional View of Through-holes in Silicon Substrate by PAECE; Broken Lines Mean Cutting Planes.

done experiments changing the following conditions.

- Changing resistivity of the substrate from 1 to 100Ω·cm
- Two different pitches of V-groove (80μm and 162.5μm)

Fig. 5 shows the dependence of TH opening diameter and the 'side-branches' depth on Si substrate resistivity at two different THs pitches. The diameter was wider according to the increase of the resistivity, also the 'side-branches' depth decreased. The TH opening diameter in an 80~120Ω·cm substrate was 3 times wider and the 'side-branches' depth was 75% less than in a 1~2Ω·cm one. Also, the narrower (80μm) TH pitch improved 13% of the depth compared to the wider (162.5μm) pitch.

This suggests that change of Space Charge Region (SCR), which is defined by the following equation (2), would dominate the phenomenon[4].

$$d = [2\varepsilon\varepsilon_0(V_D - V)/eN_D]^{1/2} \quad \cdots\cdots (2)$$

d : Distance of Space Charg Region
V_D : Diffusion Potential
N_D : Donor Concentration
ε : Dielectric Constant

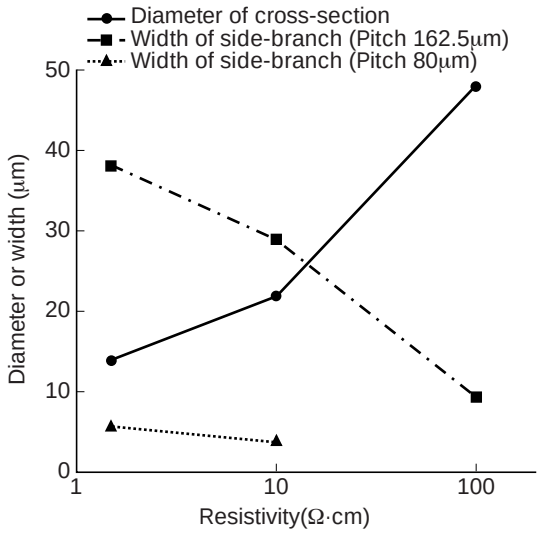

Fig. 5. Depth of 'Side-branch' and Diameter of Through-holes as Function of Si Substrate Resistivity at Two Different Through-holes Pitches.

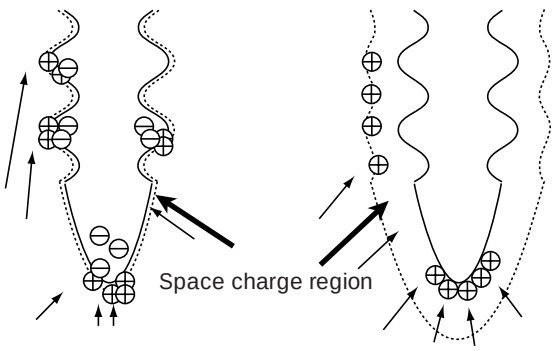

Fig. 6. Space Charge Region during PAECE.

ε_0 : Relative Dielectric Constant
e : Charge of Electron

As the applied voltage is constant, the SCR around TH expands in accordance with the decrease of the impurity concentrations. SCR in a 100Ω·cm substrate is 10 times wider than a 1Ω·cm substrate's. Fig. 6 shows the schematic image of SCR during PAECE. In the case of narrow SCR, the minority positive holes would hardly reach to the starting point of the 'side-branch'. Consequently, the 'side-branches' would be easy to grow. As SCR became wider, the etching would occur evenly in the sidewall because the minority positive holes would not reach to the starting point of the 'side-branch'. Therefore, the TH opening diameter would be wider and the 'side-branches' depth would decrease. In addition, when the TH pitch was narrower, the 'side-branches' depth would decrease because the minority positive holes would be concentrated to the bottom points of each TH.

2.2 Insulator Forming

After the THs were formed in the Si substrate, insulation layers were formed on the sidewall of THs by the thermal oxidation. The condition of oxidation was 1,100℃, 3 hours in steam. The thickness of the SiO_2 layer on both the surface of substrate and sidewall of the THs was 1.2μm, which was measured on cross sectional SEM photograph. However, other low temperature processes up to 400℃ must be required when we have to handle IC built in Si substrates. The PE-CVD would be the most possible alternative technology, but it is difficult to form reliable and thick SiO_2 layers in deep THs at this moment.

2.3 Metal Filling by MMSM[5]

Regarding methods for refilling THs with conductive material, electro or non-electroplating are typical techniques to form conductive interconnections in the THs. However, those methods cannot be applied for filling high aspect ratio THs due to the difficulties in circulation of the plating solution causing undesirable voids in the metal. Therefore, our MMSM has the advantage because of its capability to fill high aspect ratio THs without any voids. In order to fill the THs with metal, the MMSM makes use of the differential pressure between vacuum and the atmospheric pressure. The selection of the filled metal must be considered as follows;

(1) Low vaporization pressure at the melting point to perform filling operation in vacuum
(2) Low coefficient of thermal expansion to prevent the sucked metal from forming voids due to shrinking during cooling
(3) Low resistivity of metal to make low impedance

interconnection
Listed in Table 1 are several metals that we filled THs by MMSM in the experiments.

Fig. 7 shows the process flow of MMSM. In the experiments, the wafer was set in a chamber first, where was evacuated to 50Pa·abs., and then a melting bath was heated up to 330°C in case of Au-20wt%Sn solder. The wafer formed THs and insulation layer was dipped in the bath after the metal melt completely. One minute after the dipping, N_2 gas was introduced to the chamber up to atmospheric pressure, and the chamber was pressurized to 200kPa by N_2 gas subsequently. After keeping the pressure for one minute, the wafer was taken out from the chamber checking if the remaining metal on the surface had solidified. The excessive metal was removed by wiping during reheating process or wet etching. To improve the yield rate of the filling, we spattered Cr (30nm) and Au (500nm) at the opening edges of THs. And the metal overflowed THs the openings and formed interconnection lands, which were defined by the Cr/Au pattern on the surface of the Si substrate.

Fig. 8 and Fig. 9 show the cross-section views of Sn buried inside the high aspect ratio THs in a Si substrate by MMSM. In the case of Fig. 9, the THs were formed by PAECE. They sized 12μm in the diameter with the aspect ratio of 32 were completely filled without any voids. The THs shown in Fig. 9 were formed by Deep Reactive Ion Etching (DRIE). The opening diameter of them was 30μm with the aspect ratio of 14.

Table 1. Melting Points of Refilled Metals by MMSM

Metal	T_M(°C)
In	156.4
Sn	231.9
Au-Sn20(wt%)	280.0

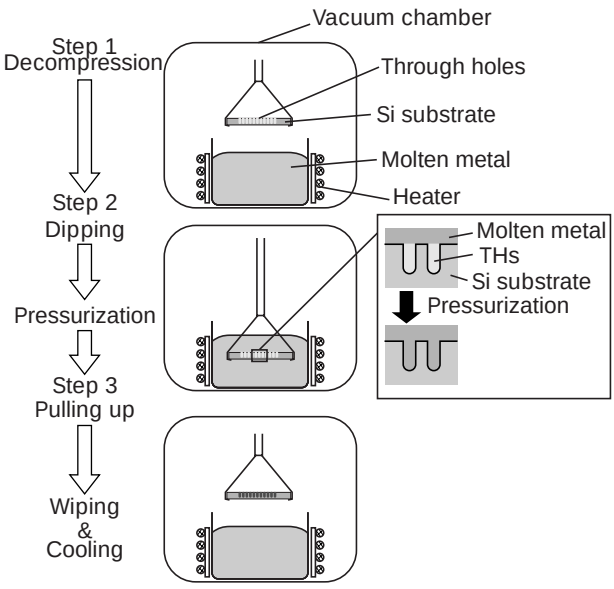

Fig. 7. Process Flow of MMSM.

3. Performances of TH Interconnections

Electrostatic micro actuators, such as micro mirror components used for the optical cross connect devices in tele- or data- communication system, have the electrodes of which are applied high voltage around 150V. When the TH interconnections are applied to those devices, high insulation resistance is required. At the same time, excellent airtightness structures of the TH interconnections to isolate from outside humidity is important.

3.1 Dielectric Breakdown Voltage

The dielectric breakdown voltage between the metal filled THs and the Si substrate of the sample shown in Fig. 9 was measured. The insulation layers were formed on the sidewall of THs by the thermal oxidation, the thickness of which was 1.2μm. As the result, the dielectric breakdown voltage was more than 500V.

3.2 Airtightness of TH Interconnections

We prepared samples shown in Fig. 10 for the air leak test. The Si substrate that had a TH interconnection was attached to a glass support by soldering. The

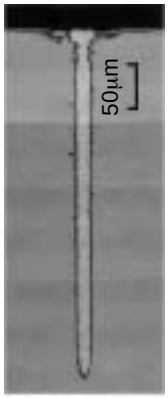

Fig. 8. Cross Sectional View of a Through-hole Interconnection in a Silicon Substrate by PAECE and MMSM.

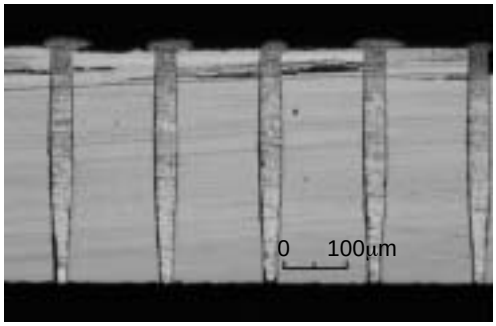

Fig. 9. Cross Sectional View of Through-hole Interconnections in a Silicon Substrate by DRIE and MMSM.

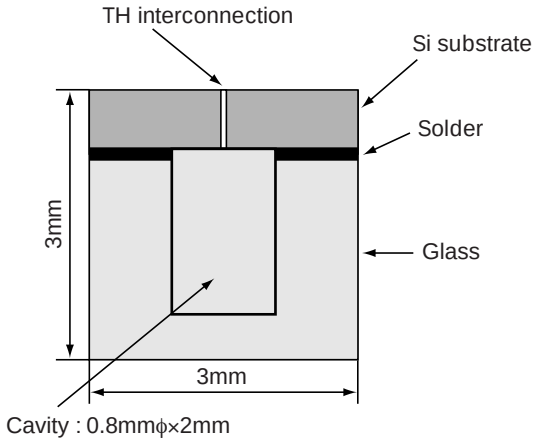

Fig. 10. Schematic Cross Sectional Illustration of a Specimen for Radioisotope Leak Test.

glass support had an internal cavity.

We did the radioisotope leak test followed by MIL-STD 883E and evaluated the airtightness of those samples. In this test, the sample was exposed to Kr-85 and dry N_2 gas in an activation chamber. If the sample had any leak paths, the Kr-85 gas soaked into the cavity through them. The soaking pressure was 2 atmospheres and the soaking time was 15 hours. After the soaking, the sample surface was washed, and the remained radioisotope in the cavity was measured with a scintillation counter.

In the result of the leak test, the sample had excellent airtightness and its leakage was lower than the detection limit (1×10^{-15}Pa·m^3/sec.).

4. Conclusion

In case of the 3D stacking of MPUs or memory modules, the back-grinding technique of Si substrates allow us to reduce the total thickness of the module after stacking. Consequently the required aspect ratio of THs interconnections for those applications has trended downward. However, the high aspect ratio TH interconnections have been still required in another applications such as imaging sensors, micro mirrors, or Si interposers for high clock LSI modules. Considering those applications, we have two newly developed technologies and have experimentally made the conductive interconnections through thick Si substrate. As the forming processes of the THs, the PAECE has been applied and its 'side-branches' was improved by controlling substrate resistivity and surplus holes. And it was demonstrated that high aspect ratio THs were filled with a certain metal by the MMSM, which had enough dielectric breakdown voltage against the substrate (more than 500V) and no-leakage between the front and the back of the substrate (less than 1×10^{-15}Pa·m^3/sec.). We will evaluate the long-term reliability of the TH interconnections and plan to develop the mass production technologies of PAECE and MMSM.

References

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